

Notice of Allowability

Application No.

09/742,036

Examiner

Leonid Shapiro

Applicant(s)

MATSUZAKI, TOSHIYUKI

Art Unit

2673

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Amendment filed on 04.28.05.
2. ☒ The allowed claim(s) is/are 14-19, 21, 22, 24, 26-27 and 28, renamed as 1-12.
3. ☒ The drawings filed on 12/20/00 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|---------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| 1. <input type="checkbox"/> Notice of References Cited (PTO-892) | 5. <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 6. <input type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date _____ |
| 3. <input type="checkbox"/> Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date _____ | 7. <input type="checkbox"/> Examiner's Amendment/Comment |
| 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| | 9. <input type="checkbox"/> Other _____ |

Allowable Subject Matter

1. Claims 14-19, 21-22, 24, 27-28 are allowed.
2. The following is an examiner's statement of reasons for allowance:
The invention concerns a module for a display device comprising:
a wiring substrate having a single level of wiring thereon;
a plurality of integrated circuits mounted on the wiring substrate in juxtaposition, each integrated circuit comprising a switching circuit having inputs coupled to n input terminals (where n is a natural number and $n \geq 2$) to receive data signals, the switching circuit generating l output signals (where l is a natural number > 2) coupled to a drive signal generation circuit for driving the display device each of the integrated circuits having the input arranged linearly in a row along a first side and the output on a second side parallel to the first side, the second side facing the display device, the first side facing away from the display device, the switching circuit sequentially connecting the first through n -th input terminals to the first through l -th output terminals respectively when a control signal is at a first logical level and sequentially connecting the first through n -th input terminals to the l -th through first output terminals, respectively when the control signal is at a second logical level;
wherein wiring on the wiring substrate is connected to the n input terminals to couple data signals to the inputs of the switching circuits, the wiring being parallel lines, and the wiring for the first integrated circuit approaches the integrated circuit on the wiring substrate from a first direction and a wiring for the second integrated circuit approaches the integrated circuit on the wiring substrate from a second direction opposite to the first

Art Unit: 2673

direction, as claimed in claim 14. The closest art, Cha et al, Mica et al. and Chen disclose related drivers, either singularly or in combination fail to anticipate or render the above underlined limitation obvious.

The invention also concerns a module for a display device comprising:

a wiring substrate having a single level of wiring thereon;

a plurality of integrated circuits mounted on the wiring substrate in juxtaposition, each integrated circuit comprising a switching circuit having inputs coupled to n input terminals (where n is a natural number and $n \geq 2$) to receive data signals, the switching circuit generating I output signals (where I is a natural number > 2) coupled to a drive signal generation circuit for driving the display device each of the integrated circuits having the input arranged linearly in a row along a first side and the output on a second side parallel to the first side, the second side facing the display device, the first side facing away from the display device, the switching circuit sequentially connecting the first through n -th input terminals to the first through I -th output terminals respectively when a control signal is at a first logical level and sequentially connecting the first through n -th input terminals to the I -th through first output terminals, respectively when the control signal is at a second logical level;

wherein wiring on the wiring substrate is connected to the n input terminals to couple data signals to the inputs of the switching circuits, the wiring being parallel lines, wherein the wiring substrate is a flexible substrate and the wiring for the first integrated circuit approaches the integrated circuit on the wiring substrate from a first direction and a wiring for the second integrated circuit approaches the integrated circuit on the wiring substrate from a second direction opposite to the first direction, as claimed in claim 18. The

closest art, Cha et al, Mica et al. and Chen disclose related drivers, either singularly or in combination fail to anticipate or render the above underlined limitation obvious.

The invention concerns a module for a display device comprising:

a wiring substrate having a single level of wiring thereon;

a plurality of integrated circuits mounted on the wiring substrate in juxtaposition, each integrated circuit comprising a switching circuit having inputs coupled to n input terminals (where n is a natural number and $n \geq 2$) to receive data signals, the switching circuit generating l output signals (where l is a natural number $l \geq 2$) coupled to a drive signal generation circuit for driving the display device each of the integrated circuits having the inputs arranged linearly in a row along a first side and the output on a second side parallel to the first side, the second side facing the display device, the first side facing away from the display device, the switching circuit sequentially connecting the first through n -th input terminals to the first through l -th output terminals respectively when a control signal is at a first logical level and sequentially connecting the first through n -th input terminals to the $l-1$ through first output terminals, respectively when the control signal is at a second logical level;

wherein wiring on the wiring substrate is connected to the n input terminals to couple data signals to the inputs of the switching circuits, the wiring being parallel lines and wiring between the n -input terminals and the switching circuit comprise a continuous line between a first terminal, an input to the switching circuit and a second input terminal, as claimed in claim 15. The closest art, Cha et al, Mica et al. and Chen disclose related drivers, either singularly or in combination fail to anticipate or render the above underlined limitation obvious.

Art Unit: 2673

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

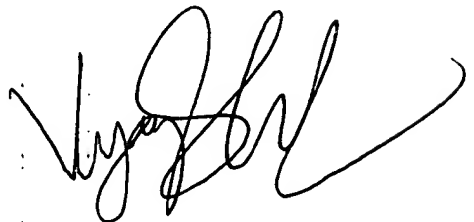
Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LS
07.18.05



VIJAY SHANKAR
PRIMARY EXAMINER